CLAIMS

1. (Original) A content addressable memory cell comprising:

a first bit line;

a second bit line;

a pair of transistors arranged to store a first bit of data at a first point and a second bit of data that is the complement of the first bit of data at a second point;

a first transistor coupled to the first bit line and the first point;

a second transistor coupled to the second bit line and the second point;

a word line coupled to the first transistor and second transistor, the word line carrying a voltage changed in accordance with process parameters to allow current conduction of the first and second transistors that compensates for leakage by the pair of transistors;

a match transistor switchable to a first state in response to a first predetermined relationship between the first and second bits and third and fourth bits transmitted on the first bit line and the second bit line and switchable to a second state in response to a second predetermined relationship between the first and second bits and the third and fourth bits;

a third transistor coupling the first bit line, first point and match transistor; and

a fourth transistor coupling the second bit line second point and match transistor.

2. (Original) The cell of claim 1 wherein each of the first transistor and second transistor comprises a low voltage threshold transistor.

3. (Original) The cell of claim 1 wherein each of the third transistor and fourth transistor comprises an n-channel metal oxide silicon field effect transistor (MOSFET).

4. (Original) The cell of claim 3 wherein the match transistor comprises a p-channel MOSFET.

5. (Original) The cell of claim 1 wherein the match transistor comprises a gate and an output circuit path coupled to a match line and wherein the cell further comprises a node interconnecting the gate, the third transistor and the fourth transistor.

6. (Original) The cell of claim 5 and further comprising a first precharge transistor arranged to precharge the node.

7. (Original) The cell of claim 6 and further comprising a second precharge transistor arranged to precharge the match line.

8. (Original) The cell of claim 7 wherein the first precharge transistor precharges the node so that the match transistor is cut off.

9. (Original) The cell of claim 1 wherein the first transistor is arranged to read data from the first point and is arranged to write data to the second point and wherein the second transistor is arranged to read data from the second point and is arranged to write data to the second point.

10. (Original) The cell of claim 1 wherein the cell comprises a semi-static cell, whereby chip fabrication area is reduced.

11. (Original) The cell of claim 1 wherein the cell comprises a dynamic cell, whereby chip fabrication area is reduced.

12. (Original) The cell of claim 1 wherein the word line voltage is adaptively changed in accordance with process parameters.

13. (Original) A content addressable memory cell comprising:

a word line;

a first bit line;

a second bit line;

a pair of transistors arranged to store a first bit of data at a first point and a second bit of data that is the complement of the first bit of data at a second point;

a first transistor coupled to the word line, the first bit line and the first point;

a second transistor coupled to the word line, the second bit line and the second point;

a match transistor switchable to a first state in response to a first predetermined relationship between the first and second bits and third and fourth bits transmitted on the first bit line and the second bit line and switchable to a second state in response to a second predetermined relationship between the first and second bits and the third and fourth bits;

a third transistor coupling the first bit line, first point and match transistor; and

a fourth transistor coupling the second bit line, second point and match transistor, wherein the word line voltage is changed in accordance with process parameters to cause the first and second transistors to be partially conductive to compensate for leakage by the pair of transistors.

14. (Original) The cell of claim 13 wherein each of the first transistor and second transistor comprises a low voltage threshold transistor.

15. (Original) The cell of claim 13 wherein each of the third transistor and fourth transistor comprises an re-channel metal oxide silicon field effect transistor (MOSFET).

16. (Original) The cell of claim 15 wherein the match transistor comprises a p-channel MOSFET.

17. (Original) The cell of claim 13 wherein the match transistor comprises a gate and an output circuit path coupled to a match line and wherein the cell further comprises a node interconnecting the gate, the third transistor and the fourth transistor.

18. (Original) The cell of claim 17 and further comprising a first precharge transistor arranged to precharge the node.

19. (Original) The cell of claim 18 and further comprising a second precharge transistor arranged to precharge the match line.

20. (Original) The cell of claim 19 wherein the first precharge transistor precharges the node so that the match transistor is cut off.

21. (Original) The cell of claim 13 wherein the first transistor is arranged to read data from the first point and is arranged to write data to the second point and wherein the second transistor is arranged to read data from the second point and is arranged to write data to the second point.

22. (Original) The cell of claim 13 wherein the cell comprises a semi-static cell, whereby chip fabrication area is reduced.

23. (Original) The cell of claim 13 wherein the cell comprises a dynamic cell, whereby chip fabrication area is reduced.

24. (Original) In a content addressable memory cell comprising a word line; a first bit line; a second bit line; a pair of transistors arranged to store a first bit of data at a first point and a second bit of data that is the complement of the first bit of data at a second point; a first transistor coupled to the word line, the first bit line and the first point; a second transistor coupled to the word line, the second bit line and the second point; a match transistor switchable to a first state in response to a first predetermined relationship between the first and second bits and third and fourth bits transmitted on the first bit line and the second bit line and switchable to a second state in response to a second predetermined relationship between the first and second bits and the third and fourth bits; a third transistor coupling the first bit line, first point and match transistor; and a fourth transistor coupling the second bit line, second point and match transistor, a method of allowing current conduction that compensates for leakage by the pair of transistors comprising changing the word line voltage in accordance with process parameters to make the first and second transistors partially conductive.

25. (Original) The method of claim 24, wherein said changing comprises adaptively changing the word line voltage in accordance with process parameters.

26. (Original) A memory cell comprising:

a first bit line;

a second bit line;

a pair of transistors arranged to store a first bit of data at a first point and a second bit of data that is the complement of the first bit of data at a second point;

a first transistor coupled to the first bit line and the first point;

a second transistor coupled to the second bit line and the second point; and

a word line coupled to the first transistor and second transistor, the word line carrying a voltage changed in accordance with process parameters to allow current conduction of the first and second transistors that compensates for leakage by the pair of transistors.

27. (Original) The memory cell of claim 26 wherein the memory cell comprises a content addressable memory cell.

28. (Original) The memory cell of claim 26 wherein each of the first transistor and second transistor comprises a low voltage threshold transistor.

29. (Original) The memory cell of claim 26 wherein the word line voltage is adaptively changed in accordance with process parameters.

30. (Currently Amended) The memory cell of claim 26 wherein the process parameters comprise process corners including one or more of ~~an SF~~ a slow-fast (SF) corner and ~~an FS~~ a fast-slow (FS) corner.

31. (Original) The memory cell of claim 26 wherein the process parameters comprise environmental temperatures in the range of -10 degrees C to 125 degrees C.

32. (Original) The memory cell of claim 31 wherein the current conduction is allowed while the first transistor and second transistor each is operated in a triode mode.

33. (Original) In a memory cell comprising a first bit line, a second bit line, a pair of transistors arranged to store a first bit of data at a first point and a second bit of data that is the complement of the first bit of data at a second point, a first transistor coupled to the first bit line and the first point, a second transistor coupled to the second bit line and the second point and a word line coupled to the first transistor and second transistor, a method of allowing current conduction that compensates for leakage by the pair of transistors comprising changing the word line voltage in accordance with process parameters to make the first and second transistors partially conductive.

34. (Original) The method of claim 33 wherein said changing comprises adaptively changing the word line voltage in accordance with process parameters.

35. (Currently Amended) The method of claim 33 wherein the process parameters comprise process corners including one or more of ~~an SF~~ a slow-fast (SF) corner and ~~an FS~~ a fast-slow (FS) corner.

36. (Original) The method of claim 33 wherein the process parameters comprise environmental temperatures in the range of -10 degrees C to 125 degrees C.

37. (Original) The method of claim 33 wherein the first and second transistor each is partially conductive in a triode mode of operation.

38. (Original) The method of claim 33 wherein the memory cell comprises a content addressable memory cell.